



Avery Summer 2022 Newsletter

Featured Video



Avery was happy to be invited to participate in the Rambus Design Summit – a virtual conference focused on chip and IP solutions for the data center, edge, automotive, and IoT devices. We shared our insights on the future of semiconductor technologies and how LPDDR5 delivers high bandwidth for a growing range of applications.

To see the presentation you need to register and you will have access to all the sessions. Ours was held on Tuesday, July 19 from 3 to 3:30.

[REGISTER HERE](#)

Session Description

LPDDR5 Delivers High Bandwidth for a Growing Range of Applications

Initially designed for mobile phones and laptops, the bandwidth and low power characteristics of LPDDR make it an increasingly attractive choice of memory for applications in IoT, automotive, edge computing and the data center. Fifth-generation LPDDR5 raises data rates to 6.4 Gbps and bandwidth to 25.6 GB/s for a x32 DRAM device. In this session, Rambus, and its partners OpenFive and Avery Design Systems will discuss their high-performance, high-quality, configurable LPDDR5 solution.



Customer Success Story - eTopus

“As designs move towards higher speeds, ultra-high speed SerDes IP is essential for leading edge networking, storage, 5G, and AI applications,” said Harry Chan CEO of eTopus. “Avery VIP gives us confidence that our innovations in ADC/DSP-based physical layer transceiver technology deliver superior bit error rate performance, lower latency and low power consumption while meeting standards compliance.”

Avery recently announced it has been chosen by eTopus as its verification IP solution partner for eTopus PCIe Gen 1-6 and 800G/400G Ethernet solutions and 112G SerDes IP for next-generation ASIC and Chiplet applications for high-performance computing and data center applications. Its high speed, low latency, low power connectivity IP supports leading-edge PCIe and Ethernet connectivity and uses Avery's PCI Express Verification IP (VIP) to ensure its IP is compliant prior to silicon validation.

Busy Summer of Shows

The high temperature have not slowed us down this summer. Avery Design Systems has been on the road for the past three months. Starting with the [PCI-SIG® Developers Conference](#) where we exhibited and spent two days talking about all things PCIe related. At this show we announced our work with [eTopus](#) and support for [Ucle](#). From there we headed straight to the 59th Design Automation Conference. [DAC 2022](#) in San Francisco, where we

provided updates on our Verification IP and testsuites. Most recently we finished up at the [Flash Memory Conference & Expo](#) where we made a series of announcements:

- Our new [CXL® 3.0 VIP](#) (*Avery was the first VIP provider to announce support of the latest standard)
- New [800G Ethernet VIP Co-Simulation Platform](#)
- Our work with [TenaFe](#) a SSD start-up using our NVMe®, PCIe, and AXI Verification IP
- An extension of our [partnership with Mobiveil](#) to accelerate NVMe based SSD design and verification

We Heard You!

The results are in from our recent customer survey, and we are sharing some of the insights we gained. We thank all of you who participated – we greatly appreciate the time and information you shared with us. Everyone who completed the online survey and agreed to chat with us via Zoom was entered into a drawing for an Apple Watch. After overcoming some international logistic hurdles we managed to get the Apple Watch to the lucky winner and hope he thinks of Avery every time he uses it.

While all the survey response were anonymous, we've compiled everyone's comments and input into an overall summary. Here is what we've learned are the most important factors to VIP customers:

- Timeliness in addressing the latest standards
- VIP quality and user friendliness as defined as less bugs; comprehensive and accurate testing features and easy customization
- A responsive and knowledgeable tech support team

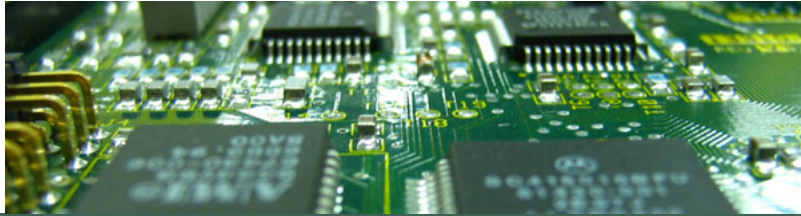
In addition to this valuable insight we learned that many of you appreciate videos and we will make sure to keep providing helpful video content.

Avery Design Systems Supports New UCIe Standard

Chiplets are the latest trend – being touted as the savior to Moore's law and the future of semiconductor design. So, of course Avery is actively supporting them. Avery announced comprehensive support for the new UCIe (Universal Chiplet Interconnect Express) standard, providing an efficient approach to enable design and verification engineers to leverage the recently introduced standard for die-to-die interface connectivity. Supporting emerging standards is key to enabling more interoperability and reducing risks associated with chiplet-based design.

[See the full News Release](#)

[See what SemiWiki has to say about it](#)



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