AVERY NEWSLETTER

LATEST NEWS FROM AVERY DESIGN SYSTEMS

June 2021

Missed us at the PCI-SIG? No problem

We have enhanced our support for the PCI standard with a solution for PCIe 6.0.
We also strengthened our partnership with Alphawave and PLDA to provide up-to-date support for the new PCIe 6.0 standard. Click on the video on the right to get an overview of our complete solution for PCIe Gen 6

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Video Showcase of the Month

The Avery PCIe 6.0 VIP solution enables advanced debug and compliance checking, and allows designers to run pre-silicon compliance testsuites.

Take a look at our CXL™ 2.0 System-level VIP Simulation Solution

Need a CXL-enabled reference system environment to verify CXL 2.0 Type 3 SoC hardware RTL and software? Check out our co-simulation solution that uses a QEMU x86 virtual host system emulator with our latest SystemVerilog CXL Host VIP.

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This Month's VIP:

After evaluating several verification IP solutions for the verification of our PCIe interfaces, we determined that Avery VIP was the best solution, allowing us to achieve our verification requirements while offering excellent capabilities and expert services and support."

Avery Design Systems and Rambus Extend Memory Model and PCIe® VIP Collaboration

The two IP companies are extending their long-term memory model and PCIe Verification IP (VIP) collaboration to enable both companies to offer fully-verified IP solutions addressing the latest market requirements.

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Save the Date: July 14. Register for a webinar on NMVe compliance

Featured partner: Astera Labs: smart retimers

We recently announced a collaboration with Aster Labs that leverages Avery's CXL 2.0 and PCIe® 5.0 Verification IP (VIP) and services in developing Astera's Aries Smart Retimer portfolio.
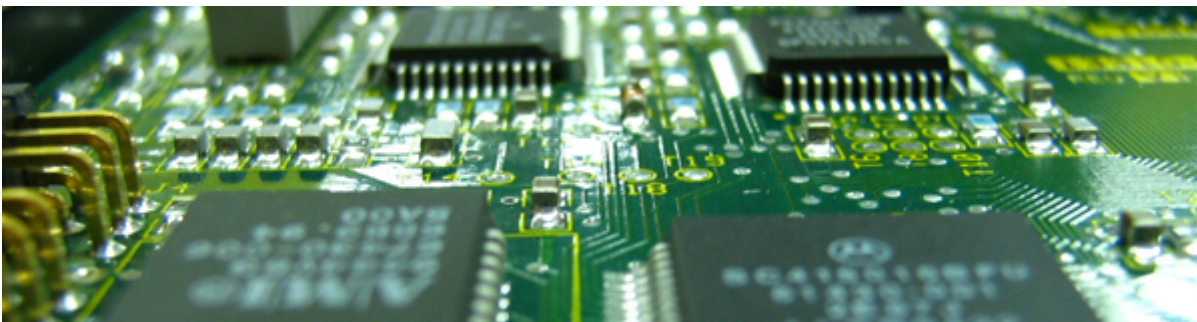
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Read about us in SemiWiki

DAC moves to December in 2021