

April 4, 2022

We want your input!

You may have already seen an email from Avery recently soliciting your input for our customer satisfaction survey – if you've already completed it – great, we thank you for taking the time to provide your feedback. If you haven't completed the survey yet – we urge you to click on the link below and complete it now. It will take less than five minutes to complete, yet this small investment of your time provides huge value to us and we hope you'll take the extra step to give us your input. We want to continue to evolve and serve you in the best way possible. Thanks in advance for clicking **HERE** and taking our survey if you haven't already. The survey closes on Friday, April 8 and so does your chance to win an iWatch.



For those of you who can be more generous with your time/input – you'll get a chance to win an Apple iWatch if you agree to conduct a brief telephone interview with our marketing agency, Wired Island International.

One final note - all responses are anonymous so you can feel free to give your honest input.

Thank you again for participating.

Click here to take our survey

Featured Video: CXL in action



"This memory pooling Proof-of-Concept (POC) video shows how CXL enables increased memory bandwidth, capacity and utilization within and across servers. Avery's comprehensive VIP enabled validation of the design prior to mapping it to the FPGA. Avery's CXL VIP was an essential element of getting the design to this point," said Supriya Madan, VP of Engineering and Co-founder at Tanzanite Silicon Solutions.

Click here to see the full video and learn how Tanzanite is enabling the next generation of composable data centers.

The demo showcases memory expansion and memory pooling across multiple servers. The lab configuration of two next generation Intel Xeon scalable processors (codenamed Sapphire Rapids) based Archer City systems, along with Tanzanite's SLICTZ SoC implemented in an Intel Agilex FPGA, was used to demonstrate 32 GB of clustered memory allocated across two hosts.

Fungible Picks Avery Design Systems PCI Express VIP for Hyperscale Compliance, Connectivity

The Fungible Data Processing Unit (DPU[™]) is an industryfirst and addresses the most challenging requirements in hyperscale data centers running data-intensive applications. Fungible selected Avery's PCI Express Verification IP (VIP) to ensure the performance of its DPU to address the demanding requirements in hyperscale data centers running dataintensive applications.

"As the industry embraces data-centric computing we are trailblazing a whole new category of microprocessor. Our silicon is front and center to how we maintain that leadership. Avery Design Systems is a leader in PCIe VIP and has been a big part of our success enabling us to consistently ensure every generation of our silicon is bug free, industry compliant and operating at the highest levels of efficiency," said Chakravarthy Kosaraju, senior vice president, silicon design and validation at Fungible.

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Expanding the Inner Circle

Avery is proud of its 20+ year history in the EDA industry and the many relationships it has cultivated over the years. While our team has worked together for many years we also value informed and objective input and appreciate the value-add our external advisors provide. We have the fortunate opportunity to have two esteemed industry leaders providing guidance on our advisory board.

Mo Movahed

As an entrepreneur, innovator and investor with a successful track record in several startups and fortune 500 companies, Mo brings relevant, first-hand experience to our advisory board. His experience leading product innovation at startups and well-established semiconductor companies along with the 15+ US Patents he hold gives him deep credibility among the team at Avery Design Systems.

Mark A. Indovina

Mark is currently the COO & Founder of Tenrehte Technologies but has been a long-term supporter of Avery Design Systems. Mark's extensive experience in the industry from established players such as Motorola and Cadence Design Systems to startups including Vivace Semiconductor and Improv Systems – Mark has a wide range of experience and knowledge to draw upon.



PCI SIG Developers Conference 2022 June 21-22, 2022 (Santa Clara, CA)



DAC 2022 July 10 – 14, 2022 (San Francisco)



Flash Memory Summit August 2 – 4, 2022 (Santa Clara, CA)

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Featured Partner



Tanzanite Silicon Solutions is a new fabless semiconductor and memory systems company creating silicon and systems for next generation datacenter design. It is a leader in the development of Compute Express LinkTM (CXLTM) based products and recently unveiled an FPGA Proof-Of-Concept vehicle demonstrating memory expansion and memory pooling, with multi-host CXL based connectivity.

Tanzanite's FPGA based demo showcases a real CXL system working across multiple servers. This is the industry's first demonstration of memory pooling, validating CXL based disaggregation and sharing of resources and showcasing Tanzanite's expertise in memory expansion and pooling.

"We are in deep engagement with industry leaders in the advancement of composable data centers leveraging the capabilities of CXL. Feedback from our prospective customers validates our leadership vision and we look forward to continuing our collaboration with CPU, memory vendors and partners, as well as customers, to accelerate the deployment of CXL based solutions for various data center use cases," stated Shalesh Thusoo, CEO, CTO and Founder of Tanzanite Silicon Solutions.

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