

USB-Xactor Test Environment

Your Solution to USB Compliance Validation



HIGHLIGHTS

- Complete solution for USB 2.0 and 3.0 core through chip-level verification
- Host, Device, Hub, PIPE/PHY models
- Compliance testsuite for Protocol, Link, and Physical layer verification of Host, Device, Hub, PHY
- Comprehensive assertions track USB compliance coverage
- Functional coverage tracks range of packet traffic, FSMs, and complex operational sequences
- Packet and symbol tracker monitor output improves debug
- Supports Verilog and SystemVerilog OVM/VMM environments
- Delivered in SystemVerilog source code
- Proven with multiple IP vendors

INTRODUCTION

The USB-Xactor supports verification of USB-based designs using the USB 3.0 standard. USB-Xactor allows users to verify their designs by developing custom tests at several levels of abstraction. USB-Xactor models support APIs from the pseudo USB Driver (USBD) and Host Controller Driver levels down to interacting directly at the protocol through physical layers. Major features supported are:

- Host performs bus enumeration and allocates independent USB pipes for communication flows between host and each device endpoint
- Program TP sequences for Bulk, Isochronous, Interrupt, Bulk Stream, and Control (Device request) transfer types
- Program USB Device requests to access USB device descriptors
- Automatic frame scheduling and bus interval and service interval support including ITP generation
- Program and send protocol layer packets
- Program USB host and device model timing parameters and response behaviors such as link commands
- Automatic flow control
- Fine-grained control over LTSSM transition sequences
- Fine-grained link layer controls
- Inject errors at all layers through callbacks
- Control device operations state transitions including suspend/resume
- Full power management support (U0-U3) including automatic and software directed entry/exit
- PowerOn and Inband reset

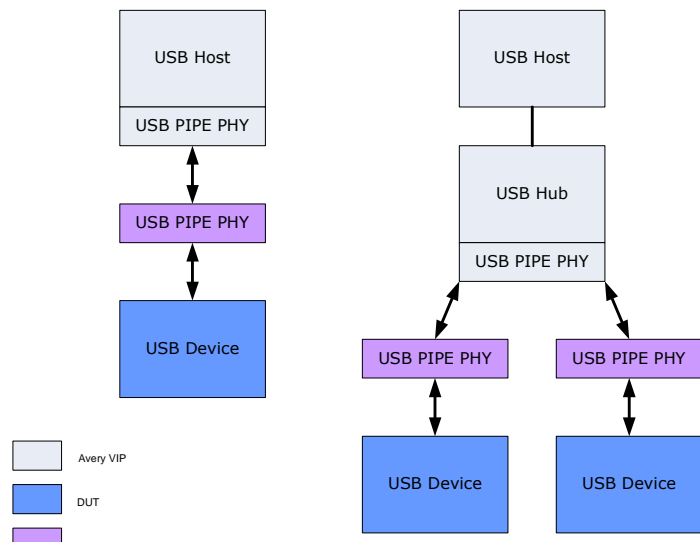


Figure 1 Sample Topologies Supported

SYSTEMVERILOG ENVIRONMENT

USB-Xactor supports an object oriented SystemVerilog testbench comprised of

- Layered environment based on family of SystemVerilog classes and methods
- Abstract data model for transfer, packet, and descriptor types
- Drivers, event callbacks, and scoreboard options to automate status and result checking
- Directed and random error injection supported through callbacks and built-in methods at various layers
- Random scenario generation with constraints stress design operation
- Directed tests for focused functional compliance testing
- Functional coverage monitoring of scenario cases
- Comprehensive protocol checking
- VMM/OVM support

CORE THROUGH CHIP-LEVEL VERIFICATION

The USB application designer can easily link the device under test into the test environment including DUT integration of the user-side logic to an USB-Xactor protocol layer model enabling full control over the DUT to initiate transactions via HCDI operations.

COMPLIANCE TEST SUITE

The test environment includes a suite of functional compliance tests. Random and directed testcases are supported. Random testing supports generating random USB transfer types and PROTOCOL/LINK/PHY layer behaviors including error injection.

PLATFORM SUPPORT

Solaris, Linux, Windows

SIMULATOR SUPPORT

Cadence	NC-SIM
Synopsys	VCS
Model Technology	Questa

LOCATIONS AND FACILITIES

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