

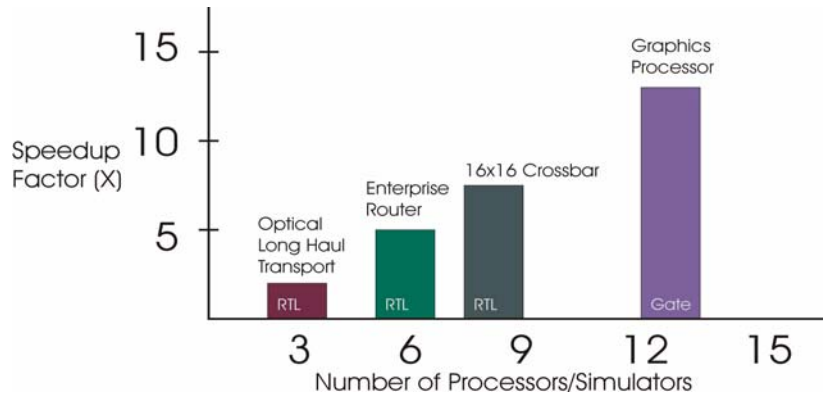
SimCluster • Parallel Simulation



Simulate Your 100 Million Gate Design on a \$10,000 PC Cluster

HIGHLIGHTS

- Increase RTL and gate-level simulation performance and capacity by 5-15 X
- Supports gate-level simulation with full SDF back-annotation
- Supports popular computing solutions of 2 to 10s of computers
- Integrated flow with popular ATPG tools for rapid validation of scan and BIST vectors
- Advanced auto-partitioning automates setup process
- Trade-off signal-level versus transaction-level accuracy for improved performance
- Works with most Verilog and VHDL simulators



OVERVIEW

Functional simulation has long been the mainstay in the functional verification of ASICs and systems. However over the last decade standalone simulator companies have not kept up with the rising functional complexity of today's SOCs and ASICs. The functional verification gap has widened to now critical proportions. Hardware accelerator and emulators offer a potential stopgap alternative to RTL functional simulation although at a price – RTL modeling restrictions, slow compile time, limited accessibility, and high economic cost.

Avery changes the status quo with innovative distributed simulation in our SimCluster solution. SimCluster unleashes the power of parallel computing for RTL and gate-level simulation and delivers scalable simulation performance of 5-15 X speedup or more. Through our multi-agent SimCluster Communication Protocol, SCP, SimCluster alleviates the performance and capacity limitations of today's standalone simulators. Our parallel simulation provides the ultimate in flexibility, openness, and scalability. SimCluster's parallel simulation runs on compute clusters as well as symmetric multiprocessors maximizing available computing resources. Now you can utilize low-cost PC cluster solutions to tackle your largest simulations configurations. SimCluster also supports popular Verilog and VHDL simulators, hardware accelerators, and emulators.

SCALABLE SIMULATION PERFORMANCE

SimCluster delivers scalable simulation performance through the parallel simulation of the sub-modules of your design. Today's SOCs and ASIC –based systems can often be partitioned at functional subsystem boundaries for distributed simulation purposes. Benchmarks have shown a 5X speedup using just 6 processors. Furthermore, distributed simulation virtually eliminates the physical memory space restrictions of today's PCs and workstations.

FLEXIBLE DISTRIBUTED COMPUTING

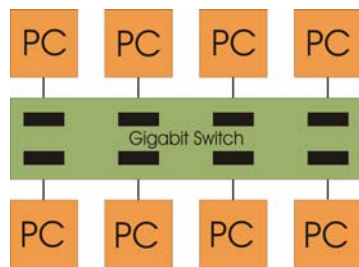
SimCluster's distributed simulation runs on the most popular computing solutions including compute clusters and symmetric multiprocessors from 2 to 10s of processors. Compute clusters require high-speed dedicated LANS (subnets) to attain maximum throughput such as 1 gigabit and 10 gigabit ethernet networks.

OPEN SOLUTION SUPPORTS POPULAR SIMULATORS

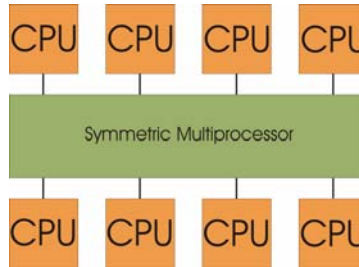
Avery's distributed simulation solution works with most Verilog and VHDL simulators on the market that are compliant with the PLI 1.0 and FLI standards. This means that you can maximize your simulation capacity and throughput as you start to run SimCluster's scalable distributed simulation. In addition, SimCluster is compatible with many hardware accelerators and emulators that support co-simulation via a PLI/FLI interface. This means that SimCluster works with all your existing solutions. Avery protects your existing investments in tools and methods.

DISTRIBUTED SIMULATION SUPPORTS VERILOG, VHDL, C/C++

Today's SOCs and embedded systems integrate 3rd party and proprietary hardware and software. System-level verification requires integration of these models into an overall simulation model. Often models come in the form of HDLs, ANSI C/C++, or specialized C++ class libraries such as SystemC. Avery's distributed simulation supports a heterogeneous environment enabling all model types to be integrated and simulated in a distributed environment.



Linux Cluster



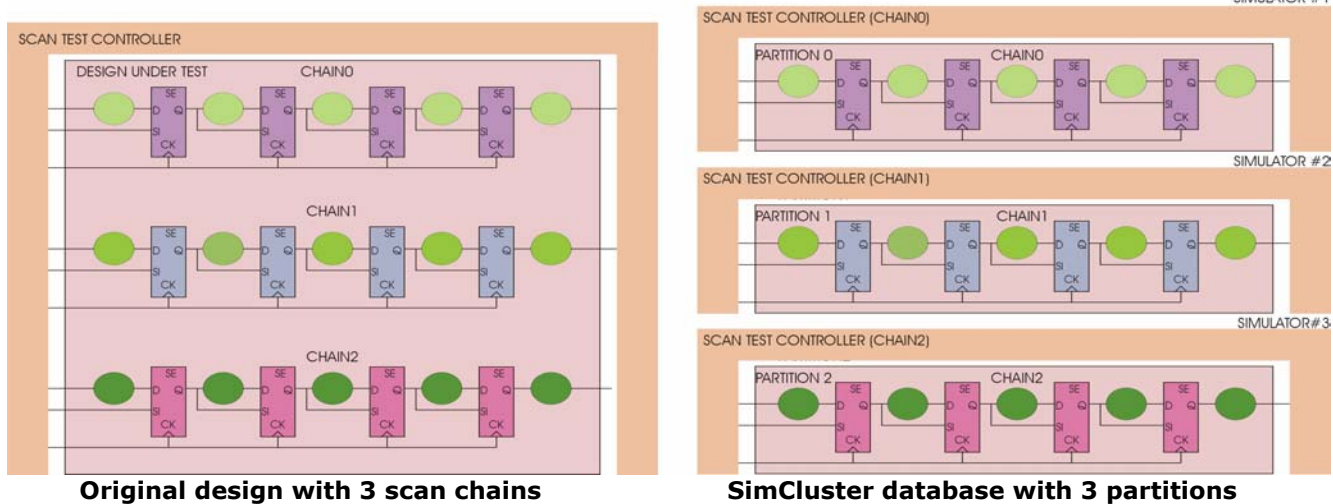
Linux or Sun SMP

EASY PARTITIONING AND SETUP

SimCluster supports an easy plug'n'play setup method for auto-partitioning Verilog designs and simulation. Partitioning a design for distributed simulation is typically done at functional subsystems boundaries. Multiple configurations can be designated and selected at runtime based on the number of compute resources available. At the gate-level, SimCluster can partition designs netlists which are flat or hierarchical. SimCluster also supports partitioning design netlist layout delay information in SDF format making SimCluster the only acceleration solution available today for speeding up full timing gate-level simulation. SimCluster also supports multiple levels of simulation synchronization accuracy to tune performance including delta-cycle, clock-based, and transactional synchronization. Simulation is fully deterministic. Avery provides diagnostic support to gauge the simulation efficiency of different partitioning scenarios.

INTEGRATED WITH ATPG SOLUTIONS

SimCluster has integrated with popular ATPG tool flows to accelerate scan vector validation. SimCluster partitions the ATPG-generated testbench and design netlist including SDF based on scan chain groups. This approach yields optimal performance by minimizing the communications overhead of parallel scan load, unload, and compare steps. Benchmarks has been shown to cut the turn around time of scan validation by more than 10X.



Original design with 3 scan chains

SimCluster database with 3 partitions

LICENSING

Every SimCluster license supports up to 3 distributed processes not including the SimCluster Manager. This means that with one SimCluster license you can simulate up to a 3-way distributed parallel simulation using popular simulators such as VCS, NC-SIM, Verilog-XL, and ModelSim.

PLATFORM SUPPORT

Solaris 32/64, Linux 32/64

SIMULATOR SUPPORT

Cadence	Verilog-XL	NC-SIM
Synopsys	VCS	
Model Technology	ModelSim	

LOCATIONS AND FACILITIES

U.S. Headquarters: 2 Atwood Lane, Andover, MA 01810, Tel: 978 689 7286, Fax: 978 258 5889

International Field Office: 5F, No. 95, Sec. 1, Chong-Qing S. Rd., Taipei, 100, Taiwan, Tel: 886-2-23817029

Sales

Avery Sales and Support

Saphirus

Facet EDA Solutions (faceteda.com)

HiTechEDA, Inc. (hitecheda.com)

BlackForest EDA (blackforest-eda.de)

Terasoft, Inc (terasoft.com.tw)

978 689 7286

408 625 7618

888 883 2238

301 915 0221

+49-2132-137485

+886-(3) 611 5678

(West)

(New England, New York)

(South)

(Europe)

(Taiwan)

WEBSITE: <http://www.avery-design.com>

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